REMARKS

In the non-final Office Action, the Examiner rejects claims 1-21 under 35 U.S.C. § 102(e) as anticipated by NATARAJ et al. (U.S. Patent No. 6,757,779).

By way of the present amendment, Applicants cancel claim 17 without prejudice or disclaimer and amend claims 1, 9, 16, and 21 to improve form. Claims 1-16 and 18-21 remain pending.

Pending claims 1-16 and 18-21 stand rejected under 35 U.S.C. § 102(e) as allegedly anticipated by NATARAJ et al. Applicants respectfully traverse.

A proper rejection under 35 U.S.C. § 102 requires that a single reference teach every aspect of the claimed invention either explicitly or impliedly. Any feature not directly taught must be inherently present. See M.P.E.P. § 2131. Applicants respectfully submit that NATARAJ et al. does not disclose or suggest the combination of features recited in claims 1-16 and 18-21.

For example, independent claim 1 is directed to a central processing unit (CPU) that includes an arithmetic logic unit; and a ternary content addressable memory operatively coupled to the arithmetic logic unit within the CPU and configured to perform one or more matching operations. NATARAJ et al. does not disclose or suggest this combination of features.

For example, NATARAJ et al. does not disclose or suggest an arithmetic logic unit. The Examiner relies on NATARAJ et al.'s priority logic 410 as allegedly corresponding to an arithmetic logic unit (Office Action, pg. 3). Applicants disagree.

NATARAJ et al. discloses that priority logic 410 compares priority numbers for all corresponding priority statements that match an incoming packet (col. 8, lines 60-63). NATARAJ et al. does not disclose or suggest that priority logic 410 is an arithmetic logic unit, as arithmetic logic unit is commonly known in the art. Instead, NATARAJ et al.'s priority logic

410 appears to be a single function device and not, as required by claim 1, an arithmetic logic unit. If this rejection is maintained, Applicants request that the Examiner identify where in NATARAJ et al. it is disclosed that priority logic 410 is an arithmetic logic unit.

NATARAJ et al. does not further disclose a ternary content addressable memory operatively coupled to the arithmetic logic unit within the CPU and configured to perform one or more matching operations. The Examiner alleges that NATARAJ et al.'s ternary CAM 404 corresponds to this feature of Applicant's claim 1 (Office Action, pg. 3). Applicants respectfully disagree.

NATARAJ et al. discloses that ternary CAM 404 is part of a classification system 400 of a policy-based router (Fig. 4; col. 7, lines 38-49). NATARAJ et al. in no way discloses or suggests, however, that ternary CAM 404 is operatively coupled to an arithmetic logic unit within a CPU, as required by amended claim 1. NATARAJ et al. does not disclose or suggest that classification system 400 is a CPU. Moreover, as set forth above, NATARAJ et al. does not disclose an arithmetic logic unit. Therefore, NATARAJ et al. cannot disclose ternary CAM 404 being connected to an arithmetic logic unit.

For at least the foregoing reasons, Applicants submit that claim 1 is not anticipated by NATARAJ et al.

Claims 2-15 depend from claim 1. Therefore, these claims are not anticipated by NATARAJ et al. for at least the reasons given above with respect to claim 1. Moreover, these claims recite additional features not disclosed or suggested by NATARAJ et al.

For example, claim 7 recites that the ternary content addressable memory is located within the arithmetic logic unit. The Examiner points to CAM array 6001 as allegedly corresponding to the recited ternary content addressable memory and CAM block 1 as allegedly implemented as an arithmetic logic unit (Office Action, pg. 3). Applicants disagree.

NATARAJ et al.'s Fig. 60 depicts a CAM device 6000 that includes multiple independently selectable CAM blocks 1-K. Contrary to the Examiner's allegation, NATARAJ et al. in no way discloses or suggests that any of CAM blocks 1-K is implemented as an arithmetic logic unit. Therefore, the disclosure of NATARAJ et al. does not support the Examiner's allegation.

If this rejection is maintained, Applicants request that the Examiner specifically point out where in NATARAJ et al. it is disclosed that CAM block 1 is implemented as an arithmetic logic unit.

For at least these additional reasons, Applicants submit that claim 7 is not anticipated by NATARAJ et al.

Amended independent claim 16 recites a feature similar to features described above with respect to claims 1 and 7. Therefore, claim 16 is not anticipated by NATARAJ et al. for at least reasons similar to reasons given above with respect to claims 1 and 7.

Claims 18 and 19 depend from claim 16. Therefore, these claims are not anticipated by NATARAJ et al. for at least the reasons given above with respect to claim 16.

Independent claim 20 recites a feature similar to a feature described above with respect to claim 1. Therefore, claim 20 is not anticipated by NATARAJ et al. for at least reasons similar to reasons given above with respect to claim 1.

Independent claim 21 recites a feature similar to features described above with respect to claims 1 and 7. Therefore, claim 21 is not anticipated by NATARAJ et al. for at least reasons similar to reasons given above with respect to claims 1 and 7.

In view of the foregoing amendments and remarks, Applicants respectfully request the Examiner's reconsideration of this application, and the timely allowance of the pending claims.

Applicants believe no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 18-1945, under Order No. BBNT-P01-128 from which the undersigned is authorized to draw.

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Respectfully submitted,

By _____

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